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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/649,051	08/27/2003	Karsten Wieczorek	2000.108400	4956	
23720	7590 01/12/2005		EXAMINER		
	, MORGAN & AMERS	STEVENSON, ANDRE C			
HOUSTON,	MOND, SUITE 1100 TX 77042		ART UNIT	PAPER NUMBER	
,			2812		
				DATE MAILED: 01/12/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
		10/649,051	WIECZOREK ET AL.			
Office Action Su	mmary	Examiner	Art Unit			
71 444 110 20 20		Andre' C. Stevenson	2812			
The MAILING DATE of t Period for Reply	his communication app	pears on the cover sheet with the	correspondence address			
THE MAILING DATE OF THIS  - Extensions of time may be available und after SIX (6) MONTHS from the mailing  - If the period for reply specified above is  - If NO period for reply is specified above  - Failure to reply within the set or extende	crite provisions of 37 CFR 1.1 date of this communication. less than thirty (30) days, a replate maximum statutory period depended for reply will, by statute in three months after the mailing	Y IS SET TO EXPIRE 3 MONTA 36(a). In no event, however, may a reply be y within the statutory minimum of thirty (30) d will apply and will expire SIX (6) MONTHS fro a, cause the application to become ABANDOI g date of this communication, even if timely fi	timely filed lays will be considered timely. om the mailing date of this communication. NED (35 U.S.C. § 133).			
Status						
1) Responsive to commun	cation(s) filed on 28 C	October 2004.				
2a) ☐ This action is <b>FINAL</b> .						
•	Since this application is in condition for allowance except for formal matters, prosecution as to the ments is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ⊠ Claim(s) <u>1-23</u> is/are per 4a) Of the above claim(s 5) ⊠ Claim(s) <u>15-22</u> is/are all 6) ⊠ Claim(s) <u>12-14</u> is/are re 7) ☐ Claim(s) is/are ol 8) ☐ Claim(s) are subj	) <u>1-11 and 23</u> is/are w owed. ected. ojected to.	ithdrawn from consideration.				
Application Papers						
Applicant may not request Replacement drawing she	that any objection to the et(s) including the correct	er. a)⊠ accepted or b)□ objected or b)□ objected or b)□ objected or b)□ objected drawing(s) be held in abeyance. Stion is required if the drawing(s) is examiner. Note the attached Office	See 37 CFR 1.85(a). objected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119						
a) ☒ All b) ☐ Some * c) ☐  1. ☒ Certified copies o  2. ☐ Certified copies o  3. ☐ Copies of the cert application from t	None of: f the priority document f the priority document ified copies of the prio ne International Burea	s have been received in Application in Application in the contraction	ation No ived in this National Stage			
Attachment(s)	12)	Λ Π I-1				
1) Notice of References Cited (PTO-89) 2) Notice of Draftsperson's Patent Dra 3) Information Disclosure Statement(s) Paper No(s)/Mail Date	wing Review (PTO-948)	4) Interview Summa Paper No(s)/Mail 5) Notice of Informa 6) Other:				

# **DETAILED ACTION Foreign Priority**

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

#### Election/Restriction

Applicant's election of Group II claims 12 through 22 in the reply filed on 10/28/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim 1 through 11 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 10/28/04.

Additionally, for clarification of the record, claim 23 is a product claim, drawn to a test structure and should have been included in Group I of the restriction requirement, mailed 10/05/04. Therefore, claim 23 has been withdrawn form further consideration as well.

### Specification

The disclosure is objected to because of the following informalities: Page 15 line 15; "structure 200" should read "structure 2".

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Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

#### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

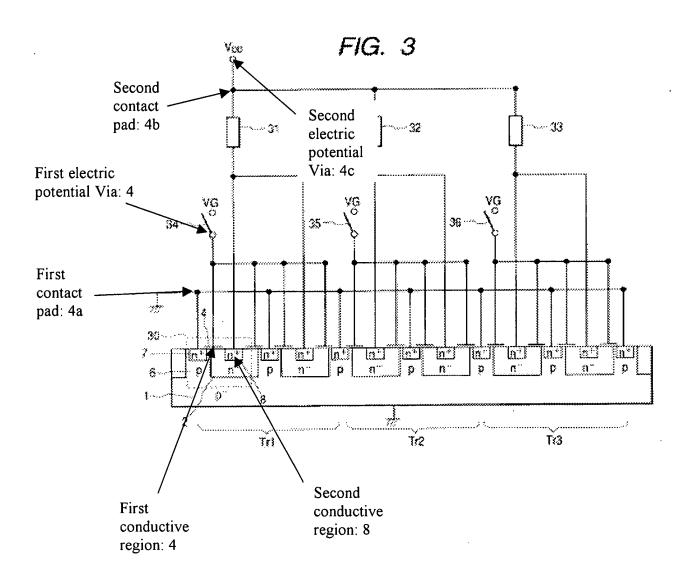
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 12 through 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimotsusa et al (U.S. Pat 6,825,543 B2)

Shimotsusa et al (U.S. Pat 6,825,543 B2), for Claim #12, shows a method, comprising: commonly connecting first conductive regions (gates) of a plurality of circuit elements (transistors) of a semiconductor structure (Fig. 3, item 2, column 10, line 10 through 13) with a first electric potential (V<sub>g</sub>) via (Fig. 3, item 4, column 11, line 29 through 33) a first common contact pad (item 4a, shown below); commonly connecting second conductive regions (item 8, drains) of said plurality of circuit elements (item Tr1) of said semiconductor structure, with a second electric potential (V<sub>DD</sub>) via (item 4c, shown below) a second common contact pad (item 4b, shown below), said first and second

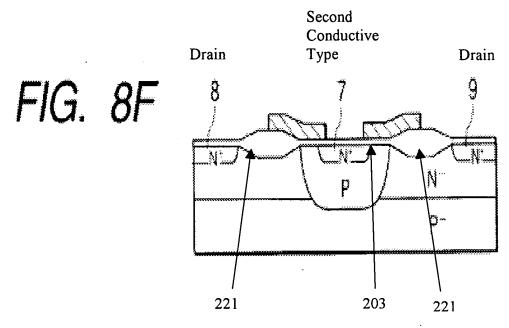
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conductive regions being insulated from each other by a dielectric (fig. 8f - 8g); and assessing a reliability of said dielectric by determining failure events of said circuit elements, (column 35, line 31 through 41, line 47 through 54).



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Field oxide (221), and gate isolation films (203) See col. 14, lines 46-55.

With respect to **Claim #13**, the method of claim 12, wherein determining said failure events includes detecting abrupt changes of a signal indicative of a dielectric breakdown of said dielectric, is taught by Shimotsusa et al (U.S. Pat 6825543 B2), (column 10, line 55 through 60).

Furthermore, **Claims #14,** The method of claim 13, wherein said signal represents a leakage current through said dielectric, is taught by Shimotsusa et al (U.S. Pat 6825543 B2), (column 10, line 55 through 67, column 16, line 1 through 7).

### **Allowable Subject Matter**

The following is an examiner's statement of reasons for allowance: While the prior art teaches a first and second common connecting well region and first and second electric potential and contact pad for their connections, it fails to teach "connecting a common well region of said plurality of transistor elements to a third electric potential by a third contact pad" and "connecting an N-well region of said at least one P-channel transistor structure to a third electric potential by a third contact pad."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claims 15 through 22 are allowable.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <a href="http://pair-direct.uspto.gov">http://pair-direct.uspto.gov</a>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866 – 217 – 9197 (toll-free).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre C. Stevenson whose telephone number is (571) 272 1683.

The examiner can normally be reached on Monday through Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (571) 272 1679. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 1782. Also, the proceeding numbers can be used to fax information through the Right Fax system;

• 703 872 9306

Andre C. Stevenson

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PRIMARY PATENT EXAMINER

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